TEXAS INSTRUMENTS

TPS54973EVM-017 9-Amp, SWIFT™ Regulator With Disabled Sink During Startup Evaluation Module

User's Guide

September 2003 *PMP Systems Power*

SLVU091

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Mailing Address:

Texas Instruments
Post Office Box 655303
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Read This First

About This Manual

This user's guide describes the characteristics, operation, and the use of the TPS54973EVM-017 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Test Setup and Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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Chapter 1

Introduction

This chapter contains background information for the TPS54973 as well as support documentation for the TPS54973EVM-017 evaluation module (HPA0017). The TPS54973EVM-017 performance specifications are given, as well as modifications.

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1.1 Background

The TPS54973EVM−017 evaluation module uses the TPS54973 synchronous buck regulator with disabled sink during startup (DSDS) to provide an output voltage from 0.9 V to 2.5 V from a nominal 3.3-V input. Rated input voltage and output current ranges are listed in Table 1−1. This evaluation module is designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54973 regulator. The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 0.6-µH output inductor.

The MOSFETs of the TPS54973 are incorporated inside the TPS54973 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs provides the TPS54973 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components are provided external to the IC and allow for an adjustable output voltage and a customizable loop response. The disabled sink during startup (DSDS) feature allows the TPS54973 regulator to be used in applications where it is necessary to prebias the output to maintain a specified difference between I/O and core voltages during startup.

Table 1−1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54973EVM−017	3.0 V to 4.0 V	−9 A to 9 A

1.2 Performance Specification Summary

A summary of the TPS54973EVM−017 performance specifications is provided in Table 1−2. Specifications are given for an input voltage of 3.3 V and an output voltage of 1.8 V unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted. The data presented in Table 1−2 was compiled with no precharge on the output (J3 open, no voltage source present on J4). Using the precharge circuitry on this EVM requires careful consideration of line and load conditions for proper operation and may limit the useful operating range of the TPS54973 device.

Table 1−2. TPS54973EVM-017 Performance Specification Summary

Parameters		Test Conditions	Min	Typ	Max	Units
Input voltage range			3.0	3.3	4.0	V
Output voltage set point				1.8		V
Output current range		V_I = 3 V to 4 V	−9		9	A
Line regulation		I_O = 4.5 A, V_I = 3 V to 4 V		±0.1%		
Load regulation		V_I = 3.3 V, I_O = 0 to 9 A		±0.3%		
Load transient response	Voltage change	I_O = 2.25 A to 6.75 A		−50		mV_{PK}
	Recovery time			160		µs
	Voltage change	I_O = 6.75 A to 2.25 A		50		mV_{PK}
	Recovery time			160		µs
Loop bandwidth		V_I = 3 V		65		kHz
Phase margin		V_I = 3 V		54		°
Loop bandwidth		V_I = 4 V		80		kHz
Phase margin		V_I = 4 V		48		°
Input ripple voltage				80	200	mV_{PP}
Output ripple voltage				6	10	mV_{PP}
Output rise time				9		ms
Operating frequency				700		kHz
Max efficiency		V_I = 3.3 V, V_O = 1.8 V, I_O = 1.5 A		92%		

1.3 Modifications

The TPS54973EVM-017 is designed to demonstrate the small size that can be attained when designing with the TPS54973, so many of the features which allow for extensive modifications have been omitted from this EVM.

1.3.1 Output Voltage

By changing the value of R_2, the output voltage can be set to a value in the range of 0.9 V to 2.5 V. The value of R_2 for a specific output voltage can be calculated by using Equation 1−1. Table 1−3 lists the values for R_2 for some common output voltages.

Equation 1−1.

$$R_2 = 10\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V}$$

Table 1−3. Output Voltage Programming

Output Voltage (V)	R_2 Value (kΩ)
0.9	1000
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49

The minimum output voltage is limited by the minimum controllable on-time of the device, 200 ns, and is dependent upon the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 1−2:

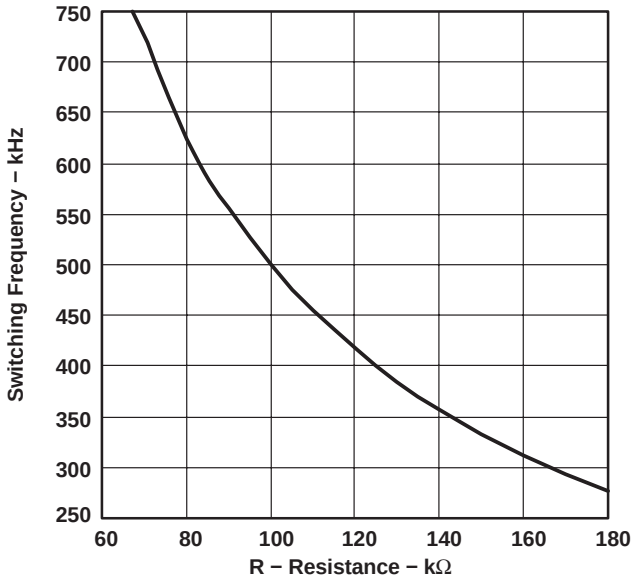
Equation 1−2.

$$V_{OUTMIN} = 200\ nsec \times f_s \times V_{INMAX}$$

1.3.2 Switching Frequency

Switching frequency can be trimmed to any value between 280 kHz and 700 kHz by changing the value of R4. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased. A plot of the value of RT versus the switching frequency is shown in Figure 1−1.

Figure 1−1. Frequency Trimming Resistor Selection Graph



1.3.3 Alternate Output Filters

The TPS54973EVM-017 EVM also supports alternate output filter configurations by means of pads located on the back side of the PCB. The positions for C15, C16, and C17 provide space for up to three electrolytic type surface mount capacitors as an alternative to the ceramic types provided. Pads for an alternate inductor at the L2 position are also included. Since changes in the output filter affect the overall loop response, the user may find it desirable to change the values used in the compensation network (R1, R3, R5, C6, C7, and C8) the 0 Ω resistor R7 in the feedback path is provided as a convenient place to break the loop for testing any compensation value changes. While the provided compensation network can provide a stable output for a wide variety of output filter component values, it is always a good idea to verify any changes to the output filter or compensation network.

1.3.4 Precharge Considerations

The primary intended usage for the TPS54973 device family is in applications requiring a precharge condition on the output. These types of applications include power supplies for DSPs and microprocessors where the I/O and core voltages must track each other within a certain amount during startup. The TPS54973 incorporates disable sink during startup to allow this type of functionality in the SWIFT family of dc/dc converters. A typical design approach is to tie the output of the core voltage to the output of the I/O voltage with a number of series diodes so that the core voltage is at a level equal to the I/O voltage minus the drop across the diodes during startup. The TPS54973EVM−017 EVM provides four series diodes, D1 through D4, and allows the user to precharge the output from either the EVM input voltage or an external source. To use the input voltage as the precharge source, install a jumper across the J3 header. To supply an external source, use the J4

connector terminals, while leaving J3 open. Headers J5 and J6 are provided to select two, three, or four series diodes. Install a jumper across the header to bypass the adjacent diode. Care must be taken to use the correct number of diodes for the application. Under no circumstances can the output voltage be allowed to precharge to a level higher than the preset output voltage. If this condition occurs during startup, the TPS54973 device does not begin switching. If a voltage transient on the precharge voltage source causes the series diodes to conduct, current may be sunk through the low side FET in the device, possibly damaging the device. The actual voltage drop across the diodes during startup depends on the initial load condition of the circuit as well as the ambient temperature.

1.3.5 Input Capacitor

An onboard electrolytic input capacitor may be added at C1.

Chapter 2

Test Setup and Results

This chapter describes how to properly connect, setup, and use the TPS54973EVM-017 evaluation module. The chapter also includes test results typical for the TPS54973EVM-017 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and startup.

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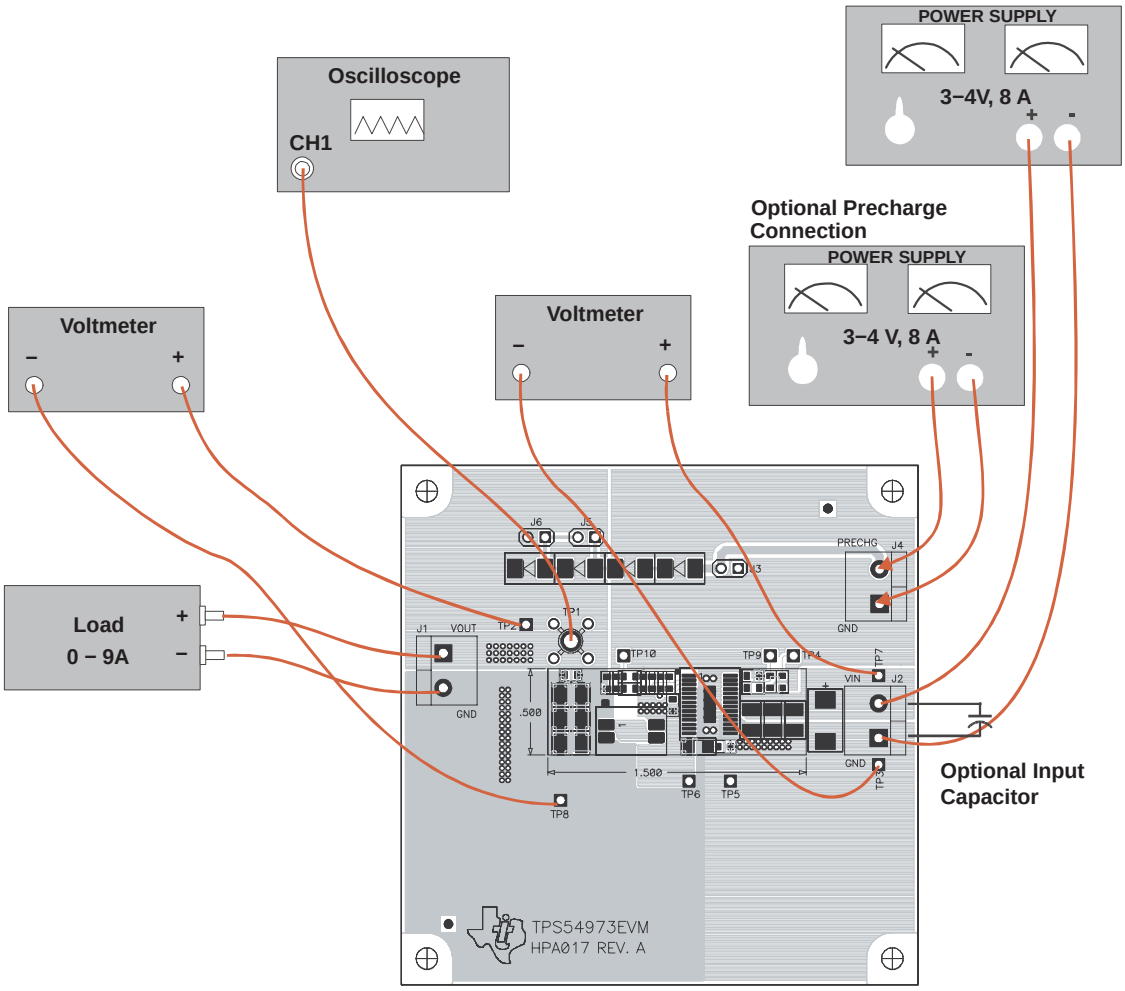
2.1 Input/Output Connections

The TPS54973EVM−017 has the following three input/output connectors: VIN J2, VOUT J1, and PRECHG_IN J4. A diagram showing the connection points is shown in Figure 2−1. A power supply capable of supplying 8 A should be connected to J2 through a pair of 20 AWG wires. The load should be connected to J1 through a pair of 20 AWG wires. The maximum load current capability should be 9 A. Wire lengths should be minimized to reduce losses in the wires. Test point TP1 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54973 is intended to be used as a point of load regulator. In typical applications it is usually located close to the input voltage source. When using the TPS54973EVM−017 with an external power supply as the source for VIN, an additional bulk capacitor may be required, depending upon the output impedance of the source and length of the hook-up wires. The test results presented were obtained using an additional 470-µF, 16-V input capacitor. Alternately, C1 may be populated with an input filter capacitor. Connection is shown for no precharge only. To utilize the precharge feature, connect the optional power supply to the J4 connector or connect the input voltage to the series diode array by inserting a jumper across the J3 header.

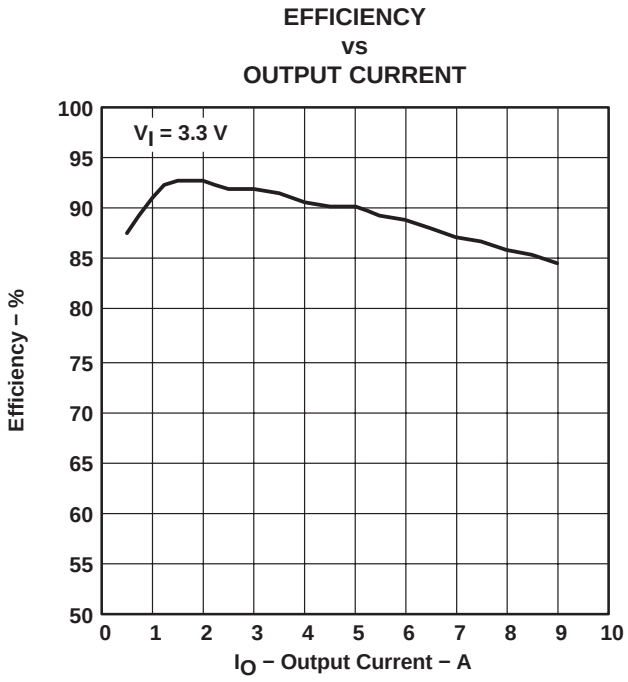
Figure 2−1. Connection Diagram



2.2 Efficiency

The TPS54973EVM−017 efficiency peaks at a load current of about 1 A to 2 A and then decreases as the load current increases towards full load. Figure 2−2 shows the efficiency of the TPS54973 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the MOSFETs. Efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

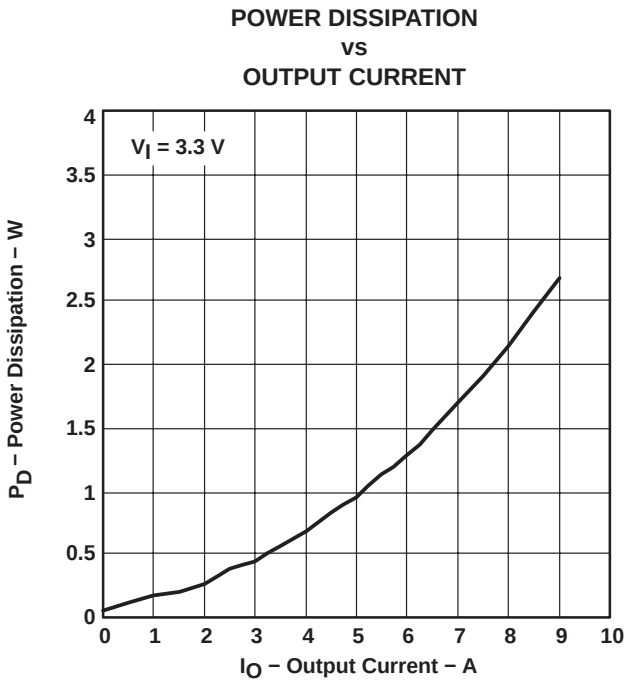
Figure 2−2. Measured Efficiency, TPS54973



2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a well designed board layout, allows the TPS54973EVM−017 EVM to output full rated load current while maintaining safe junction temperatures. With a 3.3-V input source and a 9-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C. The total circuit losses at 25°C are shown in Figure 2−3. Power dissipaton is shown for an input voltage of 3.3 V. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

Figure 2−3. Measured Circuit Losses



2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54973EVM−017 is shown in Figure 2−4, while the output voltage line regulation is shown in Figure 2−5. Measurements are shown for an ambient temperature of 25°C

Figure 2−4. Load Regulation

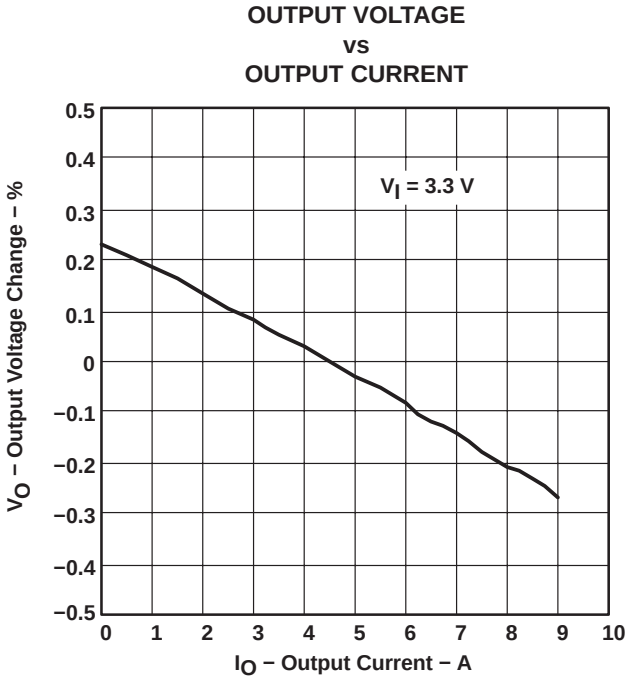
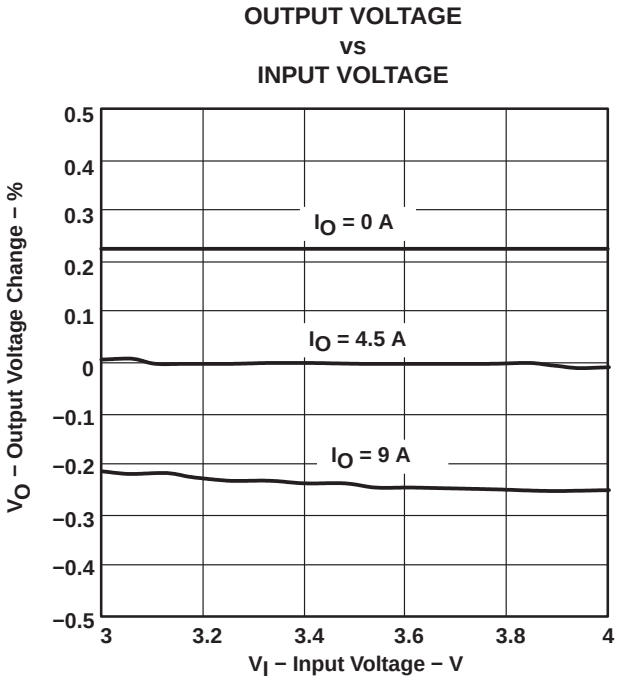


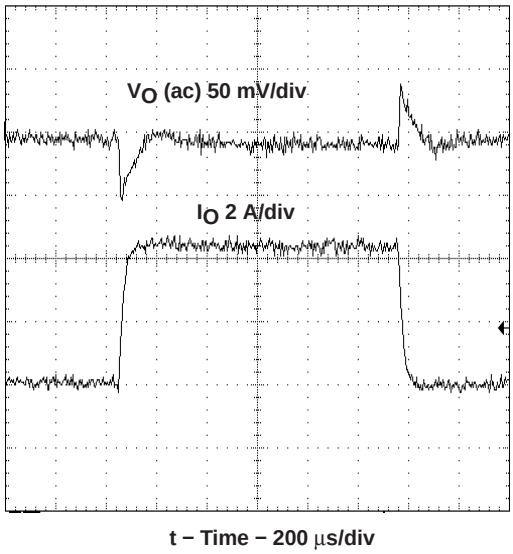
Figure 2−5. Line Regulation



2.5 Load Transients

The TPS54973EVM−017 response to load transients is shown in Figure 2−6. The current step is from 25 to 75 percent of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2−6. Load Transient Response, TPS54973



2.6 Loop Characteristics

The TPS54973EVM−017 loop response characteristics are shown in Figure 2−7 and Figure 2−8. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

Figure 2−7. Measured Loop Response, TPS54973, V_I = 3 V

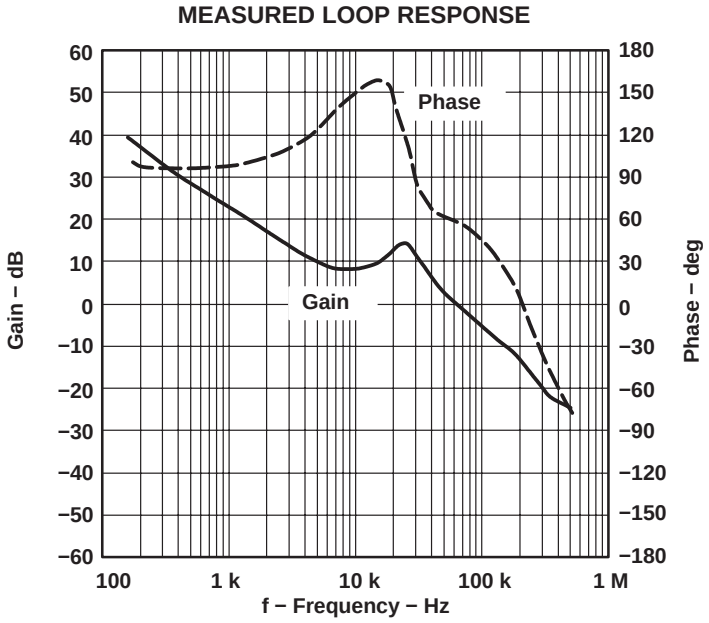
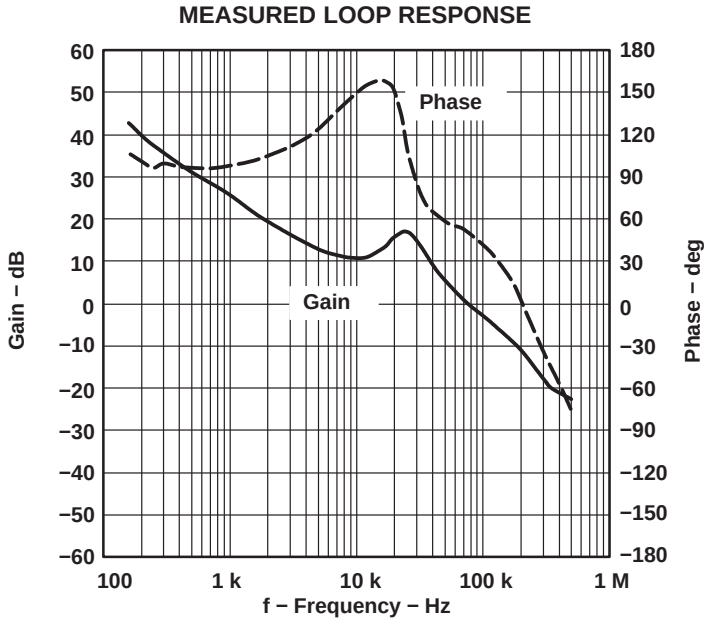


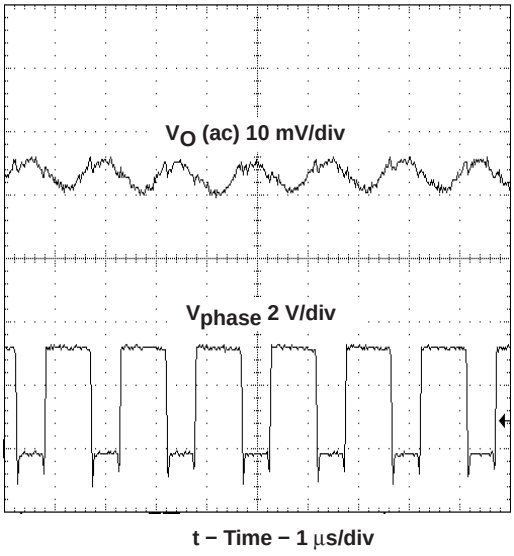
Figure 2−8. Measured Loop Response, TPS54973, V_I = 4 V



2.7 Output Voltage Ripple

The TPS54973EVM−017 output voltage ripple is shown in Figure 2−9. The input voltage is 3.3 V for the TPS54973. Output current is the rated full load of 9 A. Voltage is measured directly across output capacitors.

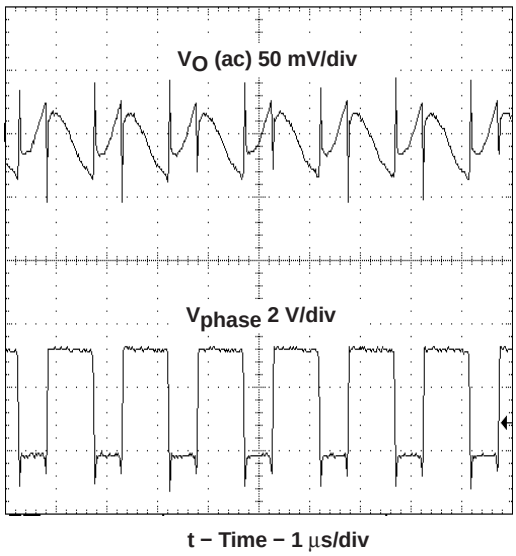
Figure 2−9. Measured Output Voltage Ripple, TPS54973



2.8 Input Voltage Ripple

The TPS54973EVM−017 output voltage ripple is shown in Figure 2−10. The input voltage is 3.3 V for the TPS54973. Output current for each device is the rated full load of 9 A.

Figure 2−10. Input Voltage Ripple, TPS54973



2.9 Start Up

The startup voltage waveforms of the TPS54973EVM−017 are shown in Figure 2−11 through Figure 2−15. Figure 2−11 shows the start up waveform with no precharge on the output. When V_I reaches the nominal 2.95-V UVLO threshold, the slow start capacitor C5 begins to charge. When the voltage on the SS/ENA pin reaches the enable threshold of 1.2 V, the internal reference begins to ramp up at the slow start rate. As the internal reference voltage increases relative to the voltage at VSENSE, the duty cycle of the PWM comparator output increases. The internal FETs are inhibited from switching until the output of the PWM comparator reaches maximum duty cycle. When maximum duty cycle is reached, switching starts and the output rises quickly while the output voltage catches up with the slow start ramp rate. At this point the voltage on the VSENSE pin matches the internal reference and the output continues to ramp up to the final set point value of 1.8 V at the slow start rate.

Figure 2−11. Measured Start Up Waveform, TPS54973 With No Precharge

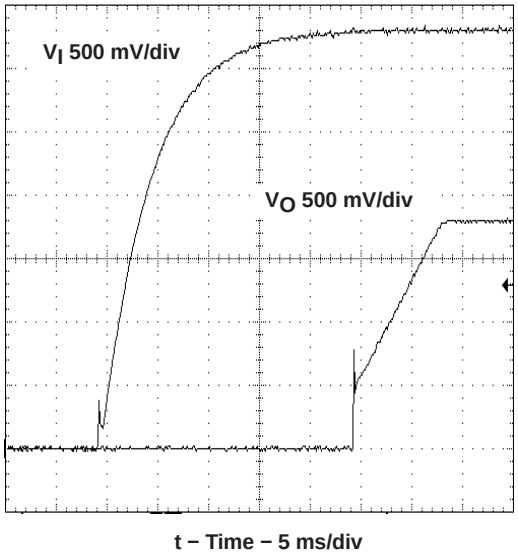


Figure 2−12 shows the start up waveform with the output precharged and a 2-Ω load. The precharge is achieved by connecting the 3.3-V input to the output with two diodes in series. The start up mechanism is the same as described above except that now the internal reference must ramp up above the voltage fed back from the precharged output to the VSENSE pin before switching can start. Once this occurs, the output continues to ramp up to the output set point of 2.5 V at the slow start rate. Figure 2−13 and Figure 2−14 show the start up waveform with three and four diodes in series. Note the different levels that the output is precharged to with 2, 3, or 4 diodes in the circuit.

Figure 2−12. Measured Start Up Waveform, Two Diode Precharge

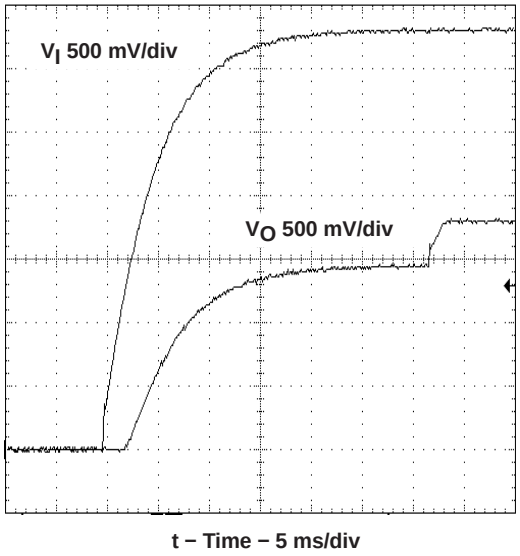


Figure 2−13. Measured Start Up Waveform, Three Diode Precharge

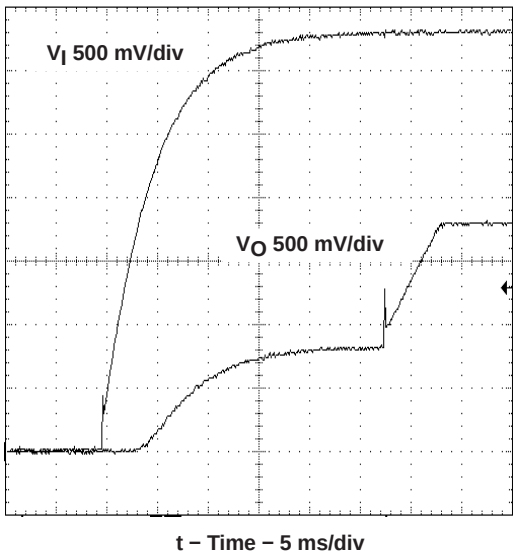


Figure 2−14. Measured Start Up Waveform, Four Diode Precharge

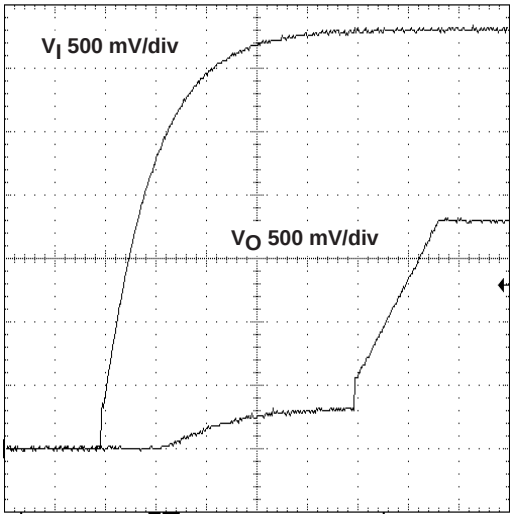
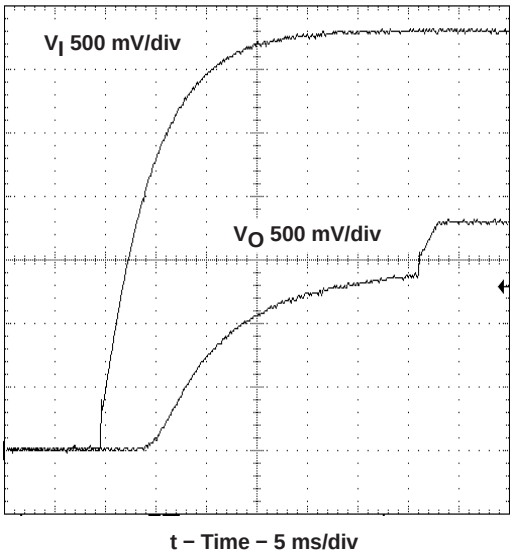


Figure 2−15 shows the start up waveform with the output precharged through four diodes and no load. Compare the precharge level to that in Figure 2−14 to see how start up load current affects the voltage drop across the diodes and the final precharge voltage. As in the previous example, when the internal reference exceeds the voltage fed back to the VSENSE pin, the output begins to ramp up to its final preset value at the slow start rate. It is important to note how the precharge level in Figure 2−15 is very close to the final output value. The precharge level must never exceed the output set point under any line or load condition for proper circuit operation. This would be the case if less than four diodes were used.

Figure 2−15. Measured Start Up Waveform, Four Diode Precharge and No Load



Chapter 3

Board Layout

This chapter provides a description of the TPS54973EVM-017 board layout and layer illustrations.

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3.1 Layout

The board layout for the TPS54973EVM−017 is shown in Figure 3−1 through Figure 3−6. The topside layer of the TPS54973EVM−017 is laid out in a manner typical of a user application. The bottom layer of the TPS54973EVM−017 is designed to accommodate optional alternate output filter capacitors. The top and bottom layers are 1.5-oz. copper.

The top layer contains the main power traces for V_I, V_O, and V_{phase}. Also on the top layer are connections for the remaining pins of the TPS54973 and a large area filled with ground. The bottom layer contains ground and V_O copper areas, some signal routing and pads for two optional D3 or D4 case size electrolytic capacitors. The top and bottom ground traces are connected with multiple vias placed around the board including 12 directly under the TPS54973 device to provide a thermal path from the PowerPAD land to ground.

The input decoupling capacitors (C9 and C10), bias decoupling capacitor (C4), and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, adjacent to the high frequency bypass output capacitor.

Figure 3−1. Top-Side Layout

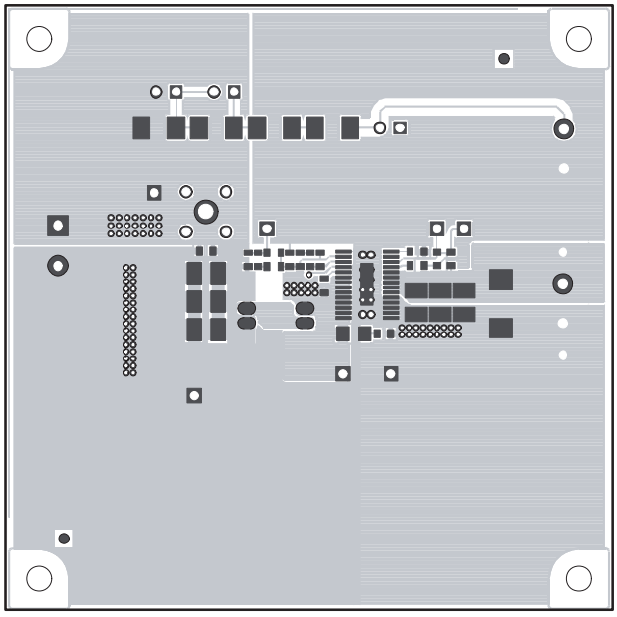


Figure 3−2. Internal Layer 2

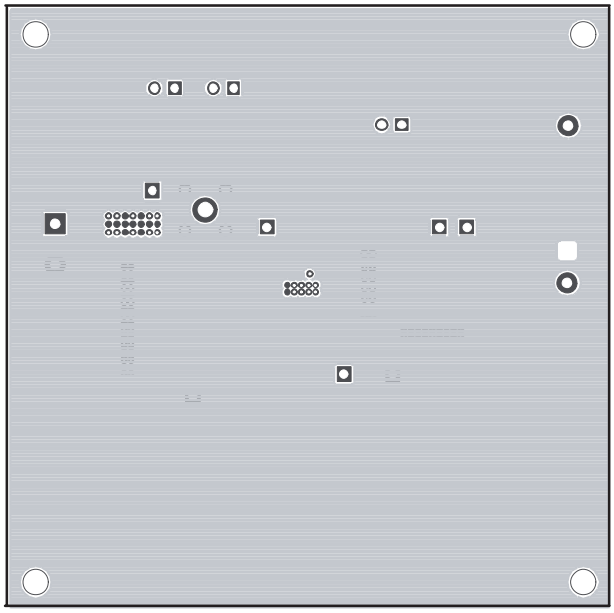


Figure 3−3. Internal Layer 3

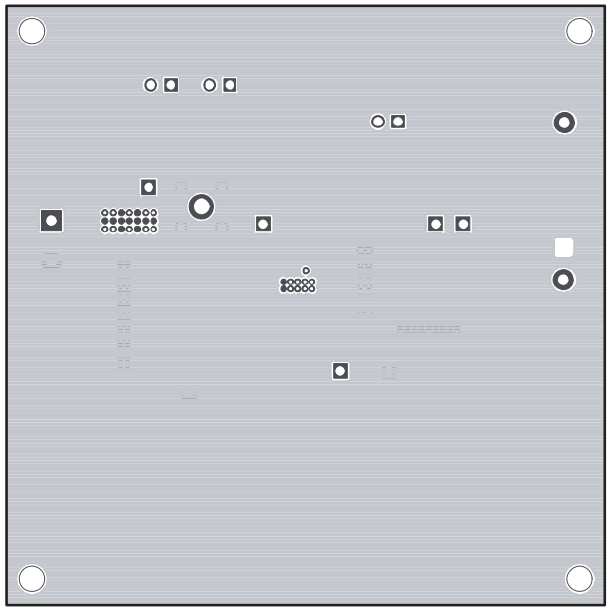


Figure 3−4. Bottom Side Layout

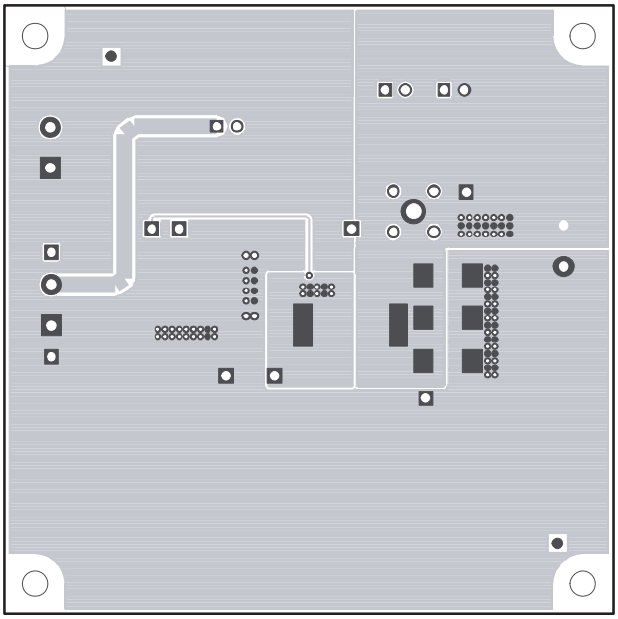


Figure 3−5. Top Side Assembly

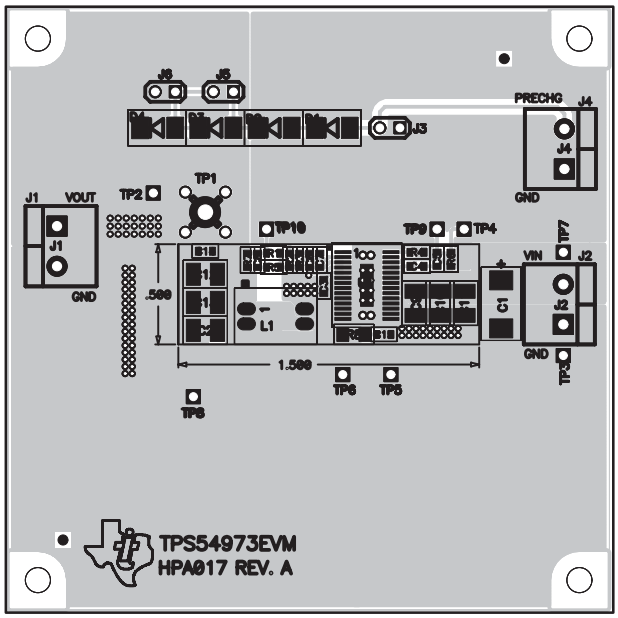
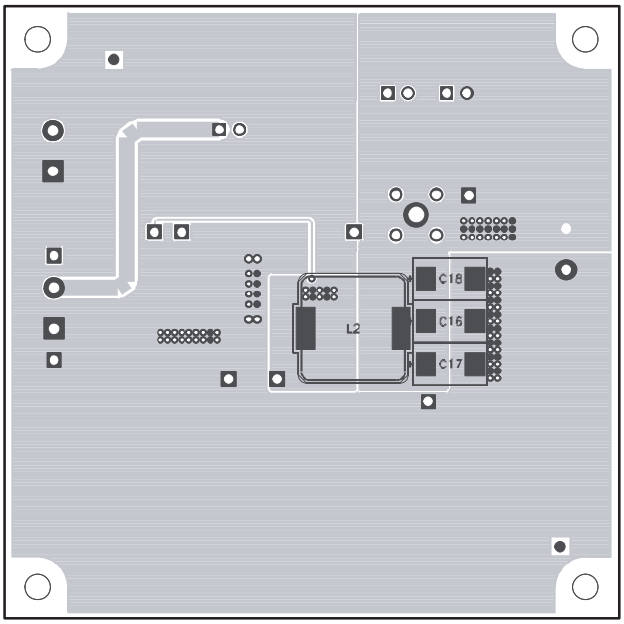


Figure 3−6. Bottom Layer Assembly



Chapter 4

Schematic and Bill of Materials

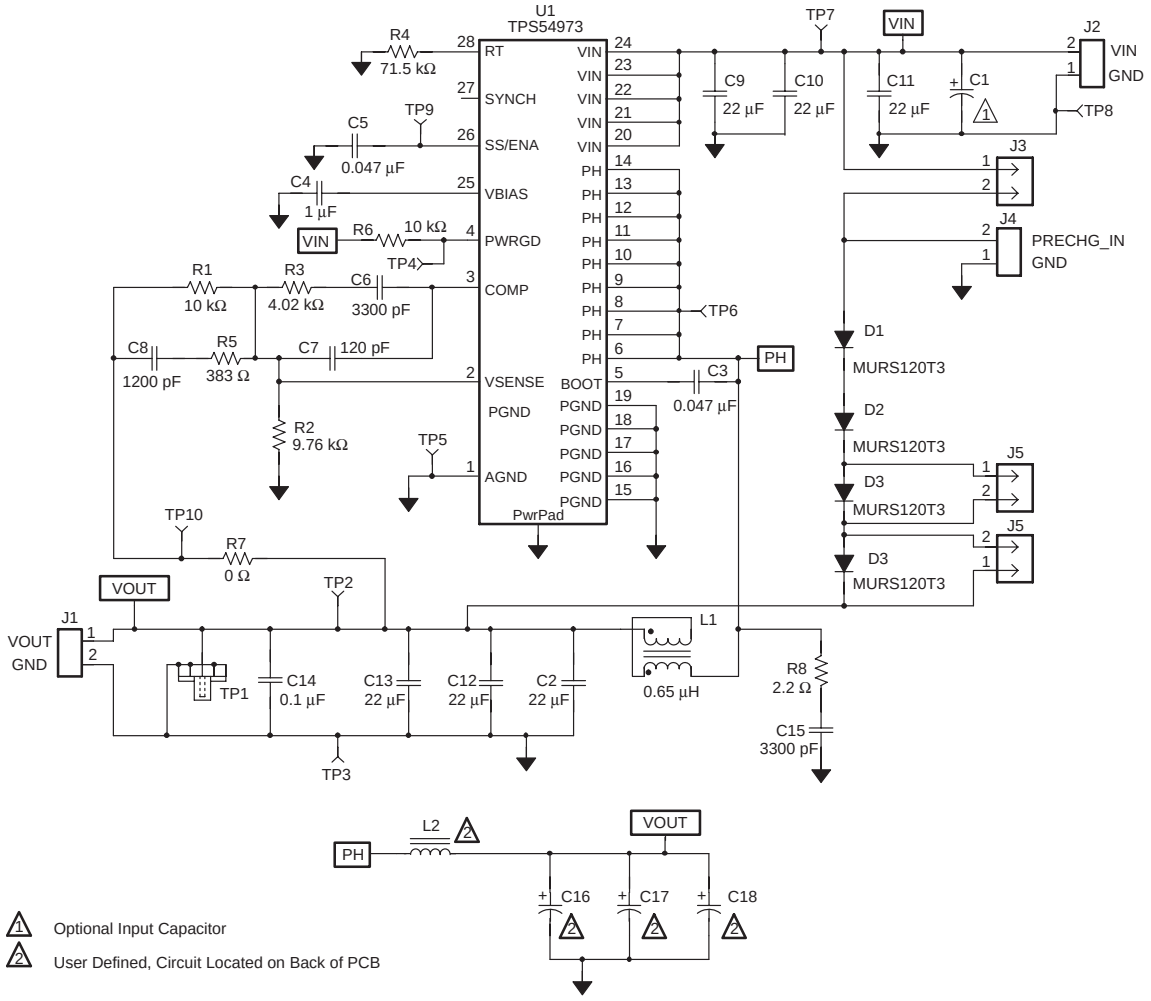
The TPS54973EVM-017 schematic and bill of materials are presented in this chapter.

Topic **Page**

4.1 Schematic

The schematic for the TPS54973EVM−017 is shown in Figure 4−1.

Figure 4−1. TPS54973EVM-017 Schematic



4.2 Bill of Materials

The bill of materials for the TPS54973EVM−017 is listed in Table 4−1.

Table 4−1. TPS54973EVM-017 Bill of Materials

Count	Ref Des	Description	Size	MFR	Part Number
−	C1	Capacitor, POSCAP, 220 µF, 10 V, 40 mΩ, 20%	7343 (D)	Sanyo	10TPB220M
1	C14	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 10%	603	Std	Std
3	C16, C17, C18	Open	62100		
6	C2, C9, C10, C11, C12, C13	Capacitor, ceramic, 22 µF, 6.3 V, X5R, 20%	1210	Taiyo Yuden	JMK325BJ226MN
2	C3,C5	Capacitor, ceramic, 0.047 µF, 25 V, X7R, 10%	603	Std	Std
1	C4	Capacitor, ceramic, 1.0 µF, 10 V, X5R, 10%	603	Std	Std
2	C6, C15	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Std	Std
1	C7	Capacitor, ceramic, 120 pF, 50 V, NPO, 5%	603	Std	Std
1	C8	Capacitor, ceramic, 1200 pF, 50 V, X7R, 10%	603	Std	Std
4	D1, D2, D3, D4	Diode, ultrafast rectifier, 1 A, 200 V	SMB	On Semi	MURS120T3
3	J1, J2, J4	Terminal block, 2 pin, 15 A, 5,1 mm	148830	OST	ED1609
3	J3, J5, J6	Header, 2 pin, 100 mil spacing, (36-pin strip)	0.100 × 2	Sullins	PTC36SAAN
3	—	Shunt, 100 mil, black	0.100	3M	929950-00
1	L1	Inductor, 0.65 µH, 12 A	0.340 × 0.250	Pulse	PA0277
1	L2	Open	0.51 × 0.51		
2	R1, R6	Resistor, chip, 10.0 kΩ, 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 9.76 kΩ, 1/16 W, 1%	603	Std	Std
1	R3	Resistor, chip, 4.02 Ω, 1/16 W, 1%	603	Std	Std
1	R4	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
1	R5	Resistor, chip, 383 Ω, 1/16 W, 1%	603	Std	Std
1	R7	Resistor, chip, 0 Ω, 1/16 W, 1%	603	Std	Std
1	R8	Resistor, chip, 2.2 Ω, 1/4 W, 1%	1206	Std	Std
1	TP1	Adapter, 3.5-mm probe clip (or 131-5031-00)	72900	Tektronix	131-4244-00
6	TP2, TP4, TP6, TP7, TP9, TP10	Test point, red, 1 mm	0.038″, 6400″	Farnell	230-345
3	TP3, TP5, TP8	Test point, black, 1 mm	0.038″, 6400″	Farnell	240-333
1	U1	IC, dc/dc converter, 3−4 V, 9 A	PWP28	TI	TPS54973PWP
1	—	PCB, 3 in × 3 in × 0.062 in		Any	HPA017

Notes: 1) These assemblies are ESD sensitive, ESD precautions should be observed.

2) These assemblies must be clean and free from flux and all contaminants, Use of no clean flux is not acceptable.

3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4) Reference designators marked with an asterisk (**) cannot be substituted. All other components can be substituted with equivalent manufacturers components.